SINGLE-PHASE MICROCHANNEL COOLING FOR STACKED SINGLE CORE CHIP AND DRAM

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ABSTRACT
The stacking of processing and memory components in a three-dimensional (3D) configuration enables the implementation of processing systems with small form factors. Such stacking shortens the interconnection length between processing and memory components to dramatically lower the memory access latencies, and contributes to significant improvements in the memory access bandwidth. Both of these factors elevate overall system performance to levels that are not realizable with prevailing and other proposed solutions. The shorter interconnection lengths in stacked architectures also enable the use of smaller drivers for the interconnections, which in turn reduces interconnection-level energy dissipations. On the down side, stacking of processing and memory components introduces a significant thermal management challenge that is rooted in the high thermal resistance of stacked designs.

This paper examines and evaluates three distinct solutions that address thermal management challenges in a system that stacks DRAM components onto a processing core. We primarily focus on three different configurations of a microchannel-based single-phase liquid cooling system with a traditional air-cooled heat sink. Our evaluations, which are intended to study the limits of each solution, assume a uniform power dissipation model for the processor and accounts for the thermal resistance offered by the thermal interface material (TIM), the interconnect layer, and through-silicon vias (TSVs). The liquid-cooled microchannel heat sink shows more promising results when integrated into the package than when added to the microprocessor package from outside.

INTRODUCTION
Technology scaling led to the miniaturization of the chip components, thereby enhancing functionality and clock rates. However, the chip interconnects did not follow the same scaling curve as the transistors and therefore became a limiting factor in performance and power consumption [1]. The electronics industry is therefore heading for 3D integration of microprocessor chips. 3D microprocessor design improves speed by decreasing interconnect length, enables smaller system form factors, and thereby reduces power dissipation and crosstalk [2]. In 3D integration, chip components are stacked vertically, which increases thermal resistances and so heat removal becomes a challenge. Because high power density, with high temperature gradients and hot spots, is already a major concern in 2D chips, reliability and performance is endangered when the electronics industry switches to 3D chips with much higher power densities.

The technology for 3D integration of the chip should be accompanied with advanced cooling solutions because conventional air cooling is ineffective for high power density circuits. Liquid cooling is a potential solution for high-temperature 3D chips owing to its high heat removal capability compared to air [3]. The ITRS 2009 also outlines liquid cooling as the most efficient cooling solution for future microprocessors. Liquid cooling is performed by attaching a heat sink with built-in microchannels and also by fabricating microchannels within the interface materials between the layers of the 3D architecture [1]. Then, a coolant (i.e., water or other fluid) is pumped through the microchannels to remove heat [1]. Explicitly, the heat is conducted from the device to the solid regions of silicon containing the microchannels where it is...
absorbed by the liquid coolant by forced convection and removed from the device [5]. High heat transfer coefficient, small mass and volume, and small coolant inventory [6] in conjunction with high materials compatibility and economical and process-compatible fabrication methodology [7] render microchannel heat sinks an excellent cooling solution. Qu and Mudawar [9] analyzed the fluid flow and heat transfer in a rectangular microchannel heat sink using water as the cooling fluid. The authors developed a numerical code based on finite difference method and used the SIMPLE algorithm to solve the governing equations. The code was verified by comparing the predictions with analytical solutions and available experimental data. The authors found a linear temperature rise along the flow direction in the solid and fluid regions of the microchannel heat sink.

A study on the effect of thermal conductivity on the heat transfer process showed that an increase in thermal conductivity of the solid substrate causes a decrease in temperature of the base surface of the heat sink, especially near the channel outlet. Li, Peterson, and Cheng [7] conducted a detailed numerical simulation of the heat transfer occurring in Silicon-based microchannel heat sinks by using a conjugate heat-transfer model considering 2D fluid flow and 3D heat transfer. A numerical code written to solve the governing equations by using a tri-diagonal matrix algorithm (TDMA) gave the detailed temperature and heat-flux distributions in the microchannel heat sink. [7] The authors studied the effect of geometric parameters of the channel and the thermo-physical properties of the fluid on the flow and heat transfer using a temperature-dependent thermo-physical property method. They stated that thermo-physical properties of the liquid significantly influence the flow and heat transfer in microchannel heat sink.

Dylan et al. [10] investigated uniformly powered microprocessor chip cooling using pressure-driven fluid flow in a microchannel heat sink. The authors analyzed the effect of width, height, and pressure drop across a channel on the cooling capability of a microchannel heat sink. They found that lower microchannels up to 100 μm in height are more effective than higher channels and the cooling capability of the heat sink is less dependent on (∆P,) across the channels.

Coskun et al. [1] provided a 3D thermal simulation model with liquid cooling that can be integrated into widely used automated thermal simulation such as HotSpot. The authors made an effort to demonstrate experimentally the efficiency of liquid cooling in reducing and balancing the temperature in a chip compared to other cooling solutions. In their work, they further coupled the liquid cooling controls with several dynamic thermal management policies to enhance the cooling efficiency. The first policy assumed a fixed flow rate and used proactive job scheduling, whereas the second policy dynamically adjusted the liquid flux to maintain temperature on the 3D stack and decrease the frequency of hot spots.

King et al. [2] for the first time worked on the configuration, fabrication, and experimental results of 3D integrated microprocessors that support the power delivery, signaling, and heat removal requirements of high-performance devices. The motivation behind this 3D integrated platform is to process and integrate the electrical and microfluidic interconnection networks at the wafer level, so that resulting chips can be assembled using flip-chip technology. The authors explain the fabrication process of the system components followed by the assembly process of these components and finally outline the testing of the system. The fabrication process takes care of the following features on a silicon die: a monolithically integrated microchannel heat sink, through-silicon electrical (copper) vias (TSEV) and through-silicon fluidic (hollow) vias (TSFV), solder bumps (electrical I/Os), and microscale polymer pipes (fluidic I/Os) on the side of the chip opposite to microchannel heat sink [2]. The assembly process discusses the flip-chip die-to-die bonding processes that enable the integration of the components in a 3D stack. The fabrication and assembly processes take into account the following issues: where to place the fluidic I/O interconnects for 3D chips, how to supply fluid to each die in a stack, and how to assemble 3D ICs to investigate the microfluidic functionality. The authors further explain the fluid delivery method applied to the 3D stack: the fluid is delivered from the top chip, through the 3D stack, and out of the bottom of the substrate with no leakage at the chip-to-chip and chip-to-substrate interfaces. The authors thus demonstrate the application of conventional flip-chip technology in the fabrication, assembly, and functionality of liquid-cooled 3D microprocessors.

Coskun et al. [3] designed an electrical system that controls the liquid flow rate in the microchannels of a microchannel heat sink and thus reduces pump energy consumption. The authors first proposed a framework that illustrates the detailed thermal modeling of the microchannels embedded in the tiers of the 3D system. The framework includes modeling of interlayer material between the tiers, TSVs, microchannels, pump, and coolant flow. A controller adjusts the liquid flow rate in microchannels dynamically to maintain a target temperature. The controller forecasts the maximum system temperature and uses its forecasts to proactively set the flow rate. The controller is also integrated with a scheduler that computes the current workload of each core as a function of the core’s thermal properties. The scheduler thus balances the temperature across the system and prevents thermal variations. Experimental results showed that combination of flow rate control and job scheduling maintain the temperature below the desired levels while reducing the cooling energy by up to 30% and achieving overall energy savings up to 12%.

Loh et al. [4] explored 3D chip stacking with an aggressive 3D DRAM organization instead of two-dimensional (2D) DRAM in which memory is stacked on the top of the microprocessor. The memory architecture is organized in a 3D environment to increase memory level parallels through a streamlined arrangement of L2 cache banks, MSHRs, memory controllers, and memory arrays. The authors introduced a novel data structure called a vector bloom filter to enable a scalable
L2 miss-handling architecture to complement the increased capacity of their 3D stacked memory system.

Kim et al. [11] numerically investigated the performance of integrated interlayer microfluidic channel cooling for 3D stacked ICs with planar and vertical non-uniform heat flux distribution. Their work quantitatively analyzed the effect of cooling mode (i.e., single-phase versus two-phase convective cooling) and geometry variation on cooling performance, thus yielding an insight and guidance on TSV scaling and electrical interconnect congestion. The work also compared the two cooling modes on the basis of effective heat transfer and pressure drop. The authors stated that dedicated hot-spot thermal management and hybrid cooling schemes combined with different cooling methods based on their power dissipation are major drivers of improved 3D IC cooling system performance by suppressing mass flow rate mal-distribution, maintaining temperature uniformity within the stack, and enhancing reliability.

This paper proposes three models of a 3D microprocessor in which DRAM components are stacked on the processing core. A liquid-cooled microchannel heat sink and finned heat sink are added to the model to cool the 3D processor components. The model also includes the interconnect layer, TIM, and TSVs to account for the thermal resistance offered by those elements and their effects on the temperature of the processor and DRAM.

**Modeling Approach**

The numerical models for the 3D stacked microprocessor considered in this study involves integration of the 2D chip, 2D memory, interconnect layer, TIM, air-cooled heat sink, TSVs, and single-phase liquid-cooled microchannel heat sink.

The computational model of the chip is approximated as a silicon cuboid of dimensions 12.5 x 13.5 x 0.2 mm. The memory in the model is also approximated as a cuboid of the same dimension. The microprocessor chip and memory are assumed to have volumetric uniform heat dissipation. The power dissipated in the chip and the memory is assumed as 100 and 20 watts respectively, for a total of 120 W. The interconnect layer is taken as cuboid of 12.5 x 13.5 x 0.015 mm [12], which takes into account the copper interconnects in the model. The TIM is assumed as a cuboid of 12.5 x 13.5 x 0.05 mm and is taken as pure Indium. The TSVs considered in this study are pure copper with via size of 0.025 mm and via pitch of 0.04 mm. The air-cooled heat sink is approximated from a commercially available heat sink [13]. This work assumes the heat sink (see Figure 1) is composed of pure aluminium and a constant convective heat transfer coefficient of 100 W/m²K is applied to it with an ambient temperature of 20ºC.

The microchannel heat sink considered in this study is inherited from Dylan et al. [8]. It has continuous channels of 12.5 mm length ($l_{ch}$), 0.1 mm width ($w_{ch}$), and 0.2 mm height ($h_{ch}$) (Figure 2). The microchannels are separated by fins 0.1 mm wide and the sidewall widths are 0.1 mm. The solid regions of the microchannel heat sink are assumed to be of silicon.

**Table 1. 3D microprocessor components description.**

<table>
<thead>
<tr>
<th>Name</th>
<th>Material and Property</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip</td>
<td>Pure Silicon</td>
<td>0.2 mm</td>
</tr>
<tr>
<td>Memory</td>
<td>Pure Silicon</td>
<td>0.2 mm</td>
</tr>
<tr>
<td>Interconnect Layer</td>
<td>Pure Copper and Silicon</td>
<td>K = 60 W/mK</td>
</tr>
<tr>
<td>Thermal Interface Material</td>
<td>Pure Indium</td>
<td>K = 86 W/mK</td>
</tr>
<tr>
<td>Heat Sink</td>
<td>Pure Aluminium</td>
<td>Convective heat transfer coefficient = 100 W/m²K</td>
</tr>
<tr>
<td>TSV Embedded in Silicon</td>
<td>K = 196 W/mK</td>
<td></td>
</tr>
</tbody>
</table>

![Figure 1. Numerical model of finned heat sink (not drawn to scale).](image1)

![Figure 2. Numerical model of the microchannel heat sink (not drawn to scale).](image2)
The fluid flow in the microchannels is assumed to be laminar and incompressible and the ambient temperature is taken as 20°C. The coolant circulating in channels is water. The fluid flow in the microchannels is assumed to be laminar and incompressible and the ambient temperature is taken as 20°C. The water enters the heat sink with uniform velocity profile, so the hydrodynamic region is included in the analysis. The no-slip boundary condition is applied on all the fluid/solid interfaces. A gauge pressure of 13.8 kPa or 2 psi is defined at the channel inlets and 0 kPa or 0 psi at the outlets. The total pressure (P_t) at any cross-section of the channel is therefore defined as the summation of the gauge pressure (i.e., the static pressure (P_{static})) at the inlet and the local dynamic pressure (P_{dynamic}), as shown in Equation 1.

\[ P_t = P_{static} + P_{dynamic} \] (1)

All the outer boundaries of the numerical model are assumed to be adiabatic. Further, heat transfer by radiation is neglected due to the very small temperature difference between the base and top surface of the model. The continuum assumption is accepted for the fluid, and Navier-Stokes equations are assumed to accurately predict the fluid flow in microchannels [6, 9, 14, and 15]. Also, the viscous dissipation term of the Navier-Stokes equations is included in the solution model [16].

The 3D microprocessor is modeled and discretized fully in both solid and fluid regions; this study accounts for the axial heat conduction and conjugate heat transfer [9]. This 3D model of a microprocessor chip with a microchannel heat sink attached to its surface is modeled in GAMBIT 2.3.16 pre-processor, and then the model is analyzed in FLUENT® 12.0.16 [17, 18], computational fluid dynamics (CFD) software. The CFD software applies the finite volume method to solve the Navier-Stokes momentum equations and the energy equations simultaneously [17, 18].

A grid-sensitivity analysis and numerical validation are performed to substantiate the resolution of discretization of the model. For this, a single microchannel comprising the complete microchannel heat sink is modeled and analyzed for the numerical solution of the Navier-Stokes and energy equations. The temperature-dependence of material properties and viscous dissipation is neglected as per the analytical solution [18] available. The discretization levels considered for grid-sensitivity analysis numbers 7,000, 20,000, 160,000, and 1,280,000 control volumes. For each of these control volumes, the Nusselt number is calculated along the length of the channel. The Nusselt number at any section of the channel having heat flux on all its four walls is defined by Equation 2.

\[ N_{u_{avg}}(x) = \frac{q'(x) \cdot d_h}{K_f \left( T_{n_{avg}}(x) - T_b(x) \right)} \] (2)

In this equation, \( N_{u_{avg}}(x) \) is the average Nusselt number at any cross section along the length of the channel, \( q'(x) \) is the average heat flux applied across the wall of the channels, \( d_h \) is the hydraulic diameter of the channel, and \( K_f \) is the thermal conductivity of the fluid. \( T_{n_{avg}}(x) \) is the axial average temperature of the perimeter of the channel and \( T_b(x) \) is the bulk fluid temperature. The bulk fluid temperature, \( T_b(x) \), is defined as

\[ T_b(x) = \frac{\int_A u \cdot T \cdot dA_c}{\int_A u \cdot dA_c} \] (3)
Figure 3 shows the variation of $\text{Nu}_{\text{avg}}(x)$ along the length of the channel. The numerical values $\text{Nu}_{\text{avg}}(x)$ are larger at the channels inlets due to the presence of the hydrodynamic region in the numerical model. On an average, the $\text{Nu}_{\text{avg}}(x)$ values for all levels of discretization converge to the thermally developed value of 3.02 [19]. The minimum percentage error for each of the four measured control volumes from fewest to most is 0.00437%, 0.00218%, 0.00129%, and 0.00056% respectively. The grid-sensitivity analysis shows the level of discretization having 7,200 control volumes sufficiently defines the fluid flow and convective heat transfer behavior in a microchannel. Thus, a complete model of the microchannel heat sink comprising 7,200 control volumes per microchannel is discretized.

Results and Discussions

The 3D microprocessor models evaluated in this study include a stacked 2D chip and DRAM. The 3D microprocessor elements such as the chip, DRAM, interconnect layer, TIM, air-cooled heat sink, and liquid-cooled microchannel heat sink are stacked to minimize temperature rise in the chip and memory. The thermal conductivity of the materials for each of the 3D microprocessor components defines the thermal resistance offered by them. The models also accounts for the thermal resistance offered by the presence of TSVs. The TSVs are assumed to exist either in the silicon fins between the channels of the microchannel heat sink or in a separate silicon-via layer added to the model. All models are analyzed at steady state and the materials properties are assumed to be constant in this study. Convective cooling by the air-cooled heat sink is accounted for by applying a constant heat transfer coefficient of 100 W/mK on the outer surface of the heat sink. Cooling by the microchannel heat sink is done by flowing the coolant (water) through the channels at a constant pressure. With 13.8 kPa and 0 kPa pressure at the inlets and outlets respectively, the Reynolds number for this flow is 159, which shows the flow is laminar.

Model-1 for the 3D microprocessor is shown in Figure 4. The origin of the Cartesian coordinates lies on lower left corner of the numerical model. As shown, the 2D chip lies at the bottom of the processor and is assumed to have uniform volumetric power dissipation of 100 W. The top of the chip has a 15-µm interconnect layer and is assumed to have thermal conductivity of 60 W/mK. The liquid-cooled microchannel heat sink is integrated over the interconnect layer and the TSVs are supposed to pass through the silicon fins separating the channels of the microchannel heat sink. The copper vias are considered to have via size of 0.025 mm, via pitch of 0.04 mm, and depth of 0.2 mm, which is same as that of the microchannel heat sink. The number of vias that can be added to the model therefore comes out to be 21,000. Because only 1D thermal conductivity along y-coordinate is considered, the thermal conductivity of the fins of the microchannel heat sink is calculated as 196 W/mK, which is the average of the thermal conductivity of copper and silicon with the proposed via size. Thus, the thermal resistance offered by the TSVs is taken into account. The cooling by microchannel heat sink occurs by fluid flowing through all the channels in $x$ direction at a constant pressure difference of 13.8 kPa. In this model, 2D DRAM lies above the microchannel heat sink with a interconnect layer of 15 µm between them. DRAM is assumed to have power dissipation of 20 W, which is uniform across its volume. The DRAM is then attached to the air-cooled finned heat sink as shown in Figure 4. The thermal resistance between the DRAM and the air heat sink is minimized by applying a 50-µm thick TIM between them. The TIM material is taken as pure Indium with thermal conductivity of 86 W/mK, which accounts for a low thermal resistance to the flow of heat from the DRAM to the air heat sink.

The coolant flowing in the channels extracts heat from the processor and there exists an axial temperature gradient in the chip, as in seen Figure 5. The temperature contours on the surface of the chip, taken at a vertical distance of 0.2 mm from the base of the chip, are shown in Figure 6(a). The highest temperature occurring on the chip’s surface is 62.9°C. The heat
dissipated in the memory also finds its way to the coolant flowing in the microchannel heat sink due to small thermal resistance offered by interconnect layer. This results in an axial temperature gradient in DRAM. The temperature contours on the surface of DRAM, taken at a vertical distance of 0.63 mm from the base of the chip, are shown in Figure 6(b). Though the highest temperature occurring on the surface of the DRAM is also 62.9°C, the volume of the DRAM having this temperature is smaller than that of the chip. As seen from the temperature contours on the surface of the memory, it can be concluded that the microchannel heat sink cools the chip efficiently and only a small amount of heat escapes to the memory, which is further taken away by the air heat sink on the top of the processor.

Model-2 proposed for the 3D processor is shown in Figure 7, in which the microchannel heat sink is supposed to be attached externally to the processor. The origin of the Cartesian coordinates is at the lower left corner of the numerical model shown in the figure, so the microchannel heat sink lies at the bottom of the proposed 3D model. The microchannel heat sink supports the TSV layer over it, which has all the TSVs passing through it. The geometrical specifications of the vias are the same as in Model-1. The number of TSVs and the thermal conductivity of the TSV layer are also the same as in Model-1 for comparison purposes. The TSV layer is followed by the 2D chip over it with a 15-µm interconnect layer between them. The power dissipation of the chip is 100 W and is distributed uniformly across the volume of the chip. The DRAM is attached directly to the chip and has power dissipation of 20 W, which is uniformly distributed across its volume. The DRAM layer is then attached to the air-cooled finned heat sink with a TIM as described in the Model-1. A constant heat transfer coefficient of 100 W/mK is applied to the air heat sink, as already discussed.

Figure 8 shows the axial gradient of temperature on the surface of the chip and DRAM. The temperature contours on the surface of the chip, taken at a vertical distance of 0.615 mm from the base of the numerical model, are shown in Figure 9(a).
The highest temperature occurring on the surface of the chip is 64.1ºC, which is 1.2 degrees higher than the chip temperature in Model-1. Moreover, by comparing Figures 6(a) and 9(a), it can be seen that the volume of the Model-2 chip with the high temperature is also larger than in Model-1. This happens because the chip in Model-2 is not placed as close to the microchannel heat sink as in Model-1. The liquid-cooled microchannel heat sink is a superior cooling mechanism to the air-cooled heat sink, and the heat escaping from the chip to the ambient in Model-2 follows a higher-thermal-resistance path than Model-1. The temperature contours on the surface of the DRAM, taken at a distance of 0.815 mm from the base of the numerical model, is shown in Figure 9(b). The highest temperature occurring on the surface of the DRAM is also 64.1ºC and there is not much difference in the volumetric heat spread of the chip and DRAM as found in Model-1. This occurs due to the direct attachment of DRAM on the chip and the lack of efficient cooling by air-cooled heat sink.

Model-3 proposed for the 3D microprocessor is shown in Figure 10. Model-3 is similar to the Model-2 except that the thickness of the TSV layer in Model-3 is twice that of Model-2. The origin of the Cartesian coordinates lies at the lower left corner of the numerical model with the microchannel heat sink at the bottom of the 3D processor. The coolant in the channels flows at same pressure difference of 13.8 kPa as in Model-1 and Model-2. The TSV layer has vias of the same diameter and pitches as in Model-1, but the depth of the vias here is 0.4 mm, which is twice that of Model-2. This increases the thermal resistance to the heat flow from the DRAM and chip to the microchannel heat sink. The 2D chip and DRAM have the same respective 100 W and 20 W power dissipation distributed uniformly across their volume. The axial variation of temperature on the surface of chip and DRAM is shown in Figure 11. The temperature contours on the surface of the chip, taken at a vertical distance of 0.815 mm from the base of the
The highest temperature on the surface of the chip is 64.5°C, which is 0.4°C higher than in Model-2. This is in accordance with the longer thermal resistance path from the chip to the microchannel heat sink. The temperature contours on the surface of the DRAM, taken at a vertical distance of 1.015 mm from the base of the numerical model, is shown in Figure 12(b). The highest temperature on the surface of DRAM is 64.5°C, which is same as that of the chip. Also, there is not much difference in the volumetric heat spread in the chip and DRAM relative to Model-2.

**CONCLUSION**

This paper proposes three models of a 3D microprocessor with advanced cooling solutions. All three models stack a 2D chip and DRAM along with a liquid-cooled microchannel heat sink and an air-cooled finned heat sink. Model-1 involves direct integration of the microchannel heat sink into the 3D processor, whereas the microchannel heat sink in Model-2 and Model-3 is added externally to enhance cooling. All models also include an interconnect layer, TIM, and TSV to account for the thermal resistance in the heat flow path. The material properties and all physical quantities involved in the models are kept constant to facilitate comparison.

This work analyzed the models on the basis of the highest temperature found on the surface of the chip and DRAM. Figure 13 graphs the temperature comparison on the surface of the chip and DRAM for the three models. The highest temperature on the surface of the chip for Model-1, Model-2, and Model-3 is found to be 62.9°C, 64.1°C, and 64.5°C respectively. This is in accordance with thermal resistance path...
from the chip to the microchannel heat sink; the path is smallest in Model-1 and largest in Model-3, while in Model-2 it lies between the two. Thus, it can be inferred that integration of the microchannel heat sink into the 3D model (as in Model-1) better cools the chip and DRAM than when it is added externally (as in Model-2 and Model-3).

As can be seen from Figure 6(b), Figure 9(b), and Figure 12(b), the volume of DRAM with the highest temperature is greater in Model-2 and Model-3 than in Model-1. This happens due to the closer proximity of the DRAM to the chip in Model-2 and Model-3 compared to Model-1. Because DRAM temperature is more critical for the function and reliability of the processor, a lower DRAM temperature is desired. Therefore, integration of the microchannel heat sink into the 3D model and separation of the DRAM from the chip assures the reliability of the high-power processors.

Thus separation of chip and DRAM as in Model-1 affects the performance of the 3D processor, but chip-DRAM proximity in Model-2 and Model-3 affects the reliability of the processor in the long run. Hence, it can be concluded that integration of the microchannel heat sink attached to the chip into the 3D microprocessor model is the more promising solution to thermal problems occurring in future high-frequency microprocessors.

**NOMENCLATURE**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>T</td>
<td>Temperature (C)</td>
</tr>
<tr>
<td>ΔP_t</td>
<td>Pressure drop across (kPa)</td>
</tr>
<tr>
<td>l_ch</td>
<td>Channel length (mm)</td>
</tr>
<tr>
<td>w_ch</td>
<td>Channel width (mm)</td>
</tr>
<tr>
<td>h_ch</td>
<td>Channel height (mm)</td>
</tr>
<tr>
<td>L</td>
<td>Length of microprocessor (mm)</td>
</tr>
<tr>
<td>W</td>
<td>Width of microchannel heat sink/processor (mm)</td>
</tr>
<tr>
<td>u</td>
<td>Fluid velocity (m/s)</td>
</tr>
<tr>
<td>d_h</td>
<td>Hydraulic diameter (m)</td>
</tr>
<tr>
<td>q''(x)</td>
<td>Heat flux at distance ‘x’ from channel inlet (W/m^2)</td>
</tr>
<tr>
<td>Nu</td>
<td>Nusselt number</td>
</tr>
<tr>
<td>Ac</td>
<td>Areas of cross-section of channel (m^2)</td>
</tr>
<tr>
<td>X</td>
<td>Axial component of Cartesian system</td>
</tr>
<tr>
<td>Y</td>
<td>Vertical traverse component of Cartesian system</td>
</tr>
<tr>
<td>Z</td>
<td>Horizontal traverse component of Cartesian system</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Subscript</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t</td>
<td>Total</td>
</tr>
<tr>
<td>avg</td>
<td>Average</td>
</tr>
<tr>
<td>w_avg</td>
<td>Average at the wall</td>
</tr>
</tbody>
</table>

**ACKNOWLEDGMENTS**

This research was supported by Semiconductor Research Corporation (SRC) under the task ID 1292.053.

**REFERENCES**


[17] ANSYS FLUENT Version 12.0.16, ANSYS Inc., Canonsburg, Penn., USA.


Estimates of stacked DRAM capacity vary from a few tens or low hundreds of megabytes \([3, 36]\) up to a few gigabytes \([20, 32]\). The OS is then responsible for deciding what memory pages should be placed in the faster, high-bandwidth stacked DRAM and what remains in conventional off-chip memory, migrating pages as necessary. Ideally, a DRAM cache hit requires only a single DRAM access latency, as shown in Figure 4(a). This is very difficult to achieve because a tag lookup is typically required to determine the actual location (i.e., physical way or column) of the requested data. Figure 4(b) shows the case in which an SRAM tag lookup provides this. Exploring Phase Change Memory and 3D Die-Stacking for Power/Thermal Friendly, Fast and Durable Memory Architectures.