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Design and Optimization of the Power Consumption in 16-bits Shift Register Using Single Edge Triggered D-Flip-Flop

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Abstract: Designing the low power devices are becoming very important field of research due to the increment of the number of portable devices. In this research, 16-bits shift register circuit design method is proposed using Single Edge Triggered (SET) D-Flip-flop. Moreover, a comparison study between the conventional circuit design and modified design is presented. The proposed circuit is designed using CEDEC 0.18 μm CMOS process. The simulated results show that SET D-FF circuit required lower power than the conventional shift register circuit. However, the conventional circuit required 16-transistors and the proposed design required 10-transistors. Therefore, 10-transistors SET D-flip-flop is the better option for 16-bits shift register.

Key words: Shift register, SET D-FF, portable applications, conventional circuit, transister

INTRODUCTION

In digital VLSI circuit design, the advanced battery using portable devices like laptops, Personal Digital Assistants (PDA), tablets and cell phones have set more targets. Portable devices become small and smaller with less space for batteries, still the necessity exists on sufficient power supply voltages. Therefore, power dissipation plays an important role in the designing of VLSI circuits (Sahu and Rincon-Mora, 2004).

Shift registers are one of the most commonly used functional devices in digital circuit systems. Most extensive uses of a shift registers are converting serial to parallel interfaces. Shift registers are useful for many circuits which work with the parallel output interfaces to convert the parallel output to serial interfaces (Akter *et al*., 2008 a, b; Reaz *et al*., 2003, 2005, 2007 a, b; Marufuzzaman *et al*., 2010). Moreover, shift registers are required for simple delay circuits. A shift registers consists of many flip-flops attached together. The inputs information are shifted from one position to either left or right depending on the kind of design of the circuit (Nagapavani *et al*., 2011). One of the most power consuming and complex circuits in the structures of shift registers blocks are flip-flops. Flip-flops consume about 30-70% of the total power of the system (Stojanovic and Oklobdzija, 1999).

Two kinds of flip-flops in shift registers Single Edge Triggered (SET) and Double Edge Triggered (DET) are widely used. The simplest flip-flops circuits are single edge-triggered which can sample data either on rising or falling clock edge only. The SET flip-flop is commonly performs as the master-slave interface. Single edge triggered D-flip-flops circuits were made to reduce the power delay or area (Reaz *et al*., 2006; Reaz and Wei, 2004; Mohd-Yasin *et al*., 2004; Mogaki *et al*., 2007; Rasouli *et al*., 2005). To reduce the area, power and delay several research have been made with a balance among these 3 areas (Hossain *et al*., 1994).

Other type of flip-flops which can be use in the shift registers are double edge triggered. In double edge triggered methods, data can be sampled on each clock edges. Moreover, SET D-flip-flops (SET D-FF) have less energy consumption than SET flip-flops. On the other hand, double-edge triggered flip-flops have bad performance when compared with single-edge circuits because of more complex circuits. In addition, most of the complexities create affect on the signal through the way (Nedovic *et al*., 2002). Flip-flops which are used in the shift registers can be static or dynamic. Dynamic flip-flop creates fault logic levels when the clocks are removed due to the fact of charge leakage from the output node capacitances. Conversely, static FF holds the output state even though the clock is removed.

In this study, 16-bits SIPO shift register with 10-transistor SET DFF design is presented with reduced area and power dissipation. The designed shift register circuit is suitable for the design of low power applications.

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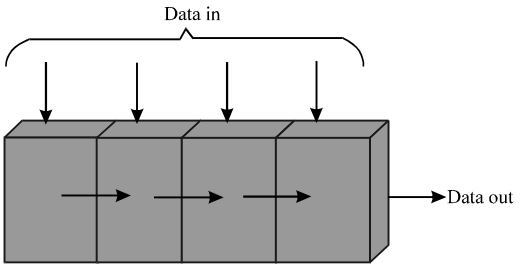

Fig. 1: Parallel in serial out block diagram

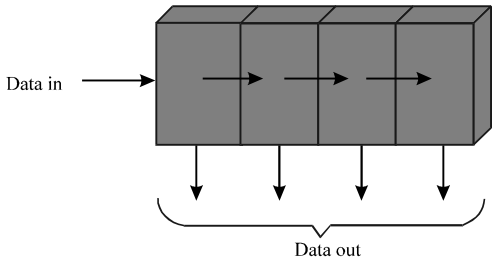

Fig. 2: Serial in parallel out block diagram

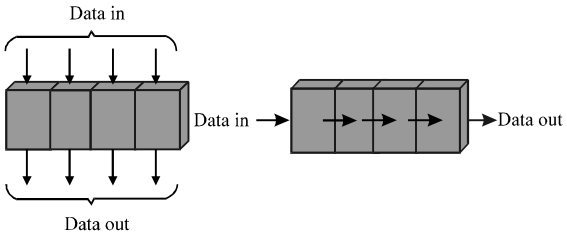

Fig. 3: Parallel in parallel out/serial in serial out block diagram

Architecture of shift register: There are different types of shift registers exists, such as Serial Input and Serial Output (SISO), Serial Input and Parallel Output (SIPO), Parallel Input and Serial Output (PISO) and Parallel Input and Parallel Output (PIPO). Parallel input serial output shift registers are commonly used to add more inputs to a microprocessor to the other devices. In PISO, each pin is interfaced to a parallel input of the shift register and the data will sent via serial to the microprocessor using several fewer inputs than originally needed (Fujiwara *et al*., 2003; He *et al*., 2010). Figure 1 shows the block diagram of the PISO shift register.

SIPO shift registers can be used to interface the output of microprocessors to the other devices when the output pins are required more than the available pins. The mechanism of SIPO helps to control many devices using only three or four pins. Figure 2 shows the block diagram of the SIPO shift register.

The other types of shifters are commonly used as a buffer on the circuits such as compact disc drives

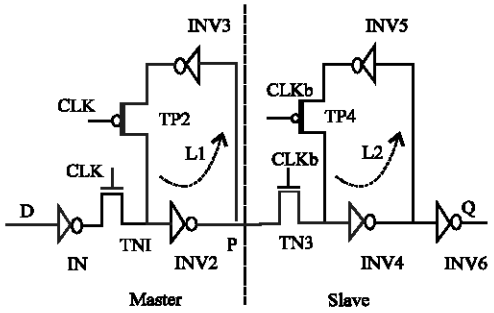

Fig. 4: Conventional 16-transistors using in the shift registers (Nogawa and Ohtomo, 1998)

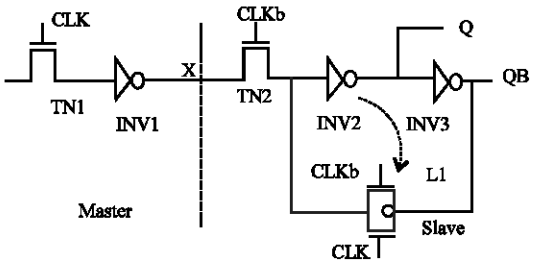

Fig. 5: Schematice diagram of the 10-T SET DFF shift register (Rasouli *et al*., 2005)

or floppy disc drives. Figure 3 shows the block diagram of the SISO and PIPO shift register. Generally, SET D-FFs are using in the structure of shift registers. Conventional 16-transistors SET D-FFs are working at both rising edge and falling edge of the clock. For the functionality of the SET D-FF, the input must be stay constant just right before setup time (t-setup) and just right after hold time (t-hold), the triggers edges of the clock. The circuit as shown in Fig. 4 shows a conventional type of 16-transistors SET D-FF. From Fig. 4, it is clear that conventional shift register operates in a master and slave parts which are determined by dashed vertical line. A PMOS transistor is used as the feedback path. In the noisy areas, pass transistors can be replaced by transmission gates.

Figure 5 shows the circuit diagram of 10-transistor (10-T) fall edge triggered SET DFF (Sharma *et al*., 2009). In this circuit, the feedback of the master part is deleted and transmission gate is included in slave feedback part. When clock is 1 master loop is in operation and the inverted data is stored in the point X. When the clock level is going to 0 the slave loop including transistor TN2 and feedback loop L1 is going to operational and generates data at the output Q and QB. When the clock is removed or grounded, the SET DFF stay in the previous level which is the main advantage of the SET D-FF. In addition, the SET D-FF is static naturally which is useful for the shift register (Sharma *et al*., 2010a).

MATERIALS AND METHODS

For the design method of 16 bits shift register, first 1-bit cell is designed to make one SET DFF. The

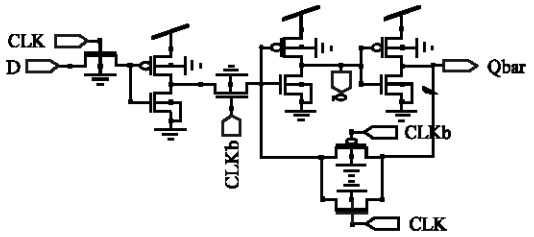

Fig. 6: Schematic diagram of the STGB bias 10-transistor (Sharma *et al*., 2010b)

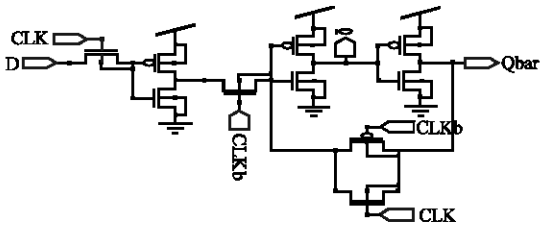

Fig. 7: NBB bias 10-transistor schematic (Sharma *et al*., 2011)

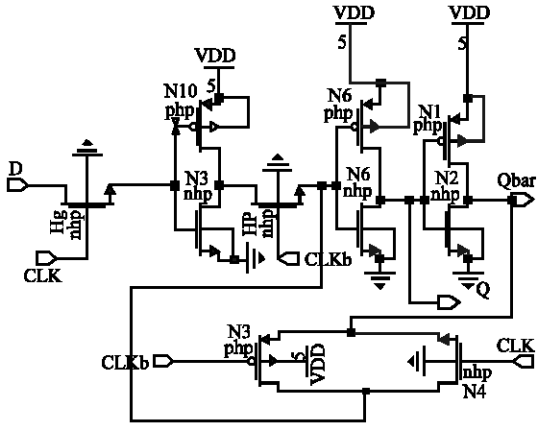

Fig. 8: Schematic diagram of 1-bit of the 16-bits shift register

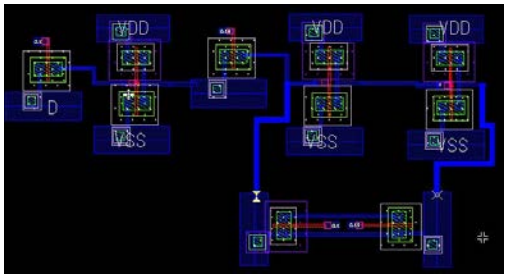

Fig. 9: The layout of one bit of 16-bits shift register

similar process has been followed to expand the design for 16-bits. In this case, two types of SET 10-transistor DFF are designed. Firstly, Sub Threshold Grounded Body (STGB) bias 10-transistor is required (Sharma *et al*., 2010a). In this kind of circuits, the body of the transistors is connected to the GND as shown in Fig. 6 with the STGB bias 10-transistor circuit.

Secondly, No Body Bias (NBB) 10-transistor SET D-FF is the required structures for the design method. In this type of circuit, the substrate of the transistors are connected to the source and thus of the transistors are always zero. Therefore, the structure is known as No Body Bias (NBB) condition (Stojanovic and Oklobdzija, 1999). Figure 7 shows the NBB 10-transistors circuit schematic diagram.

The schematic of the 1-bit DFF used in this research designed by CEDEC 0.18 μm CMOS process is shown in Fig. 8.

The modified low voltage-type 16-bits shift register layout is also designed in CEDEC 0.18 μm CMOS process as shown in Fig. 9. The 1-bit layout of the 16-bits shift register is shown in Fig. 9. For the sizing of the transistor, W/L = 0.18/0.18 μm is utilized for each CMOS transistors.

RESULTS AND DISCUSSION

CEDEC 0.18 μm CMOS process is used to measure the output results of the proposed 16-bits SET DFF shift register circuit with the ELDONET simulator. The 1.8 V power supply voltage and 27°C operating condition is used for the 16-bits SET-DFF shift register circuit design.

A comparison study of the power consumption among 16-bits shift register with 16-transistor and 10-transistor SET DFF design is shown in Table 1. It can be clearly seen from Table 1 that the power consumption of the 10-transistor circuit is less than the conventional one. Therefore, 10-transistors SET DFF design is noted in this research.

Moreover, a comparison study between the STGB and the NBB type shift register is presented in Table 2. It is obvious that the NBB shift register dissipates less power than the STGB. In addition, NBB shift register consumes lowest power among all the previous designs. Therefore, it is a better choice to design the circuit for the shift register.

Table 1: Comparison study between the proposed and conventional design

16-bits shift register using SET DFF	Power consumption
Conventional flip-flops	83.68 e^{-5}
10-transistors technology	82.08 e^{-6}

Table 2: Comparison of power consumption between STGB and NBB

Research	Power consumption (watt)
NBB (Sharma *et al*., 2011)	7.287432e-009
STGB	1.179902e-008

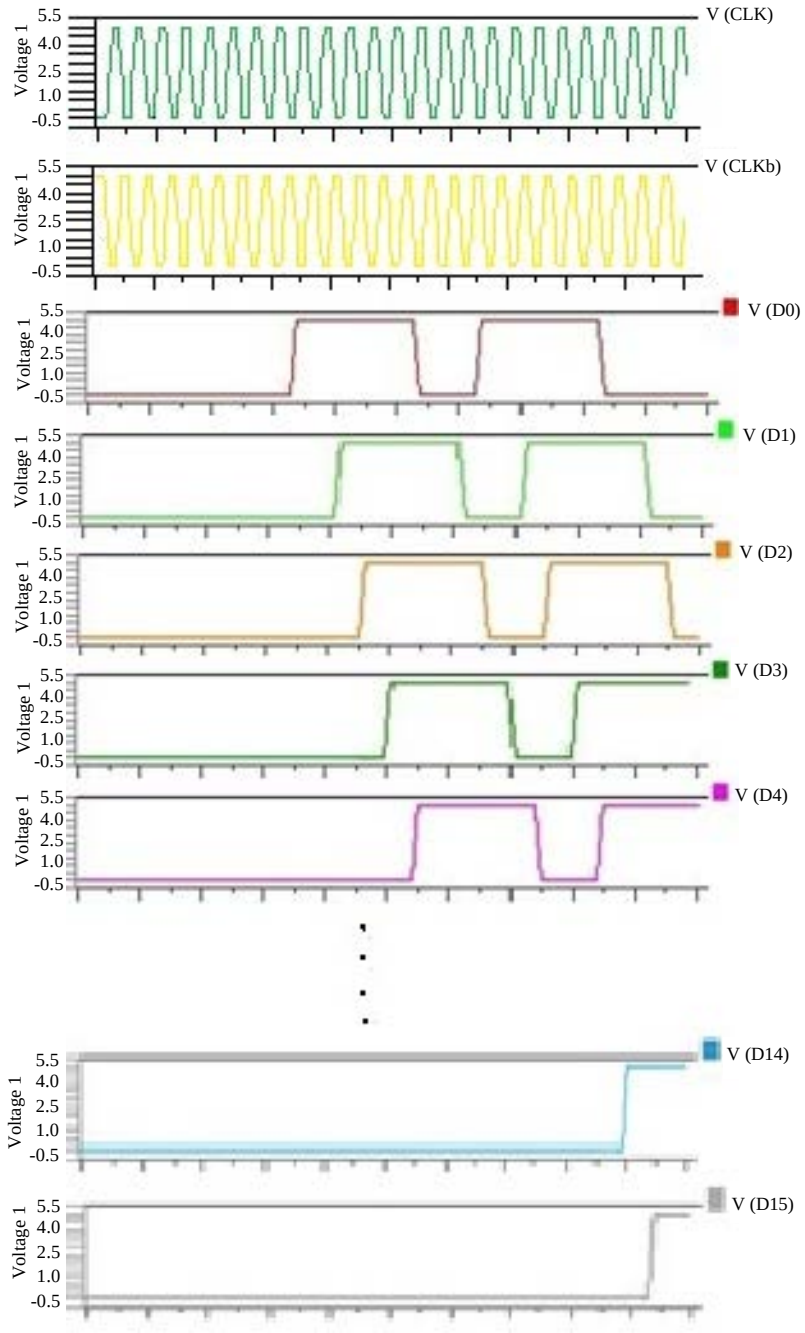

Fig. 10: The result of 16-bits shift registers using 10-transistors DFF

The simulated result of the 16-bits shift register is shown in Fig. 10. The performance of 16-bits shift register using 10-transistors DFF produce satisfactory outputs which is clearly shown in Fig. 10.

CONCLUSION

In this study, the design method of 16-bits shift register using the proposed 10-transistor SET DFF is described. In VLSI design, power consumption and area are the two major things for applicable devices. Moreover, comparison study shows that the NBB scheme for shift register circuit produced better performance in terms of power dissipation among the other designed circuits. The simulation outputs are found satisfactory using CEDEC 0.18 μm CMOS process. Therefore, among all the shift register design methods, NBB

design of negative edge triggered SET DFF circuit is suitable for power efficient portable devices.

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